HDI PCB Design Guide 2025: Mastering High-Density Interconnect Technology

Overview

High-Density Interconnect (HDI) PCBs represent the cutting edge of PCB technology, enabling smaller, faster, and more powerful electronic devices. This comprehensive guide covers HDI design principles, technologies, and best practices for 2025.

What is HDI Technology?

Definition

HDI PCBs feature:

- **Microvias**: Vias ≤0.15mm (6 mil) in diameter
- **High Via Density**: More than 600 vias per square inch
- **Multiple Lamination Cycles**: Sequential build-up layers
- **Fine Pitch**: Smaller traces and spaces
- **Passive Components**: Embedded resistors and capacitors

Applications

- **Smartphones**: Miniaturization requirements
- **Wearables**: Form factor constraints
- **Medical Devices**: Portable medical equipment
- **Aerospace/Defense**: High reliability in small packages
- **IoT Devices**: Connected, compact electronics
- **Automotive**: ADAS, infotainment systems

HDI Stack-up Designs

Type I: Single Layer Build-up

- Structure: 1+N+1
- Microvias: One side only
- Applications: Moderate density requirements
- Cost: Lower than advanced types

Type II: Double Layer Build-up

- Structure: 2+N+2
- Microvias: Both sides
- Applications: High-density designs
- Cost: Moderate

Type III: Multiple Build-up Layers

- Structure: 3+N+3 or more
- Microvias: Stacked microvias
- Applications: Very high density
- Cost: Higher

Microvia Technology

Microvia Types

Blind Microvias

- Definition: From outer layer to inner layer
- Aspect Ratio: ≤1:1 recommended
- Laser Types: CO2, UV, or hybrid

- **Applications**: Most common HDI application

Buried Vias

- **Definition**: Between inner layers only
- **Process**: Created during lamination
- **Applications**: High-density interconnects
- **Visibility**: Not visible from outer layers

Stacked Microvias

- **Definition**: Multiple microvias aligned vertically
- **Complexity**: Requires precise alignment
- **Applications**: Ultra-high density
- **Cost**: Higher due to complexity

Microvia Dimensions

Via Type	Minimum Diameter	Minimum Pad	Land	Aspect Ratio
Laser Microvia	0.075mm (3 mil)	0.20mm (8 mil)	0.25mm (10 mil)	≤1:1
Mechanical Microvia	0.15mm (6 mil)	0.30mm (12 mil)	0.40mm (16 mil)	≤0.8:1

Design Guidelines

Trace and Space

Layer Type	Minimum Trace	Minimum Space	Application
External (Type I)	0.075mm (3 mil)	0.075mm (3 mil)	Standard HDI
External (Type II)	0.05mm (2 mil)	0.05mm (2 mil)	Advanced HDI
Internal	0.075mm (3 mil)	0.075mm (3 mil)	All types

Via-in-Pad Design

Benefits

- Shorter Connections: Reduced inductance
- Space Savings: No via escape routing needed
- Better Signal Integrity: Minimizes stubs
- Thermal Performance: Better heat dissipation

Process Steps

1. Drill microvia
2. Plate via
3. Fill with epoxy (conductive or non-conductive)
4. Cure epoxy
5. Planarize surface
6. Plate over
7. Pattern and etch outer layer

BGA Escape Routing

BGA Pitch	Recommended HDI Type	Via Size	Trace/Space
≥1.0mm	Standard PCB	0.3mm	0.15/0.15mm
0.8mm	Type I HDI	0.15mm	0.1/0.1mm
0.65mm	Type II HDI	0.10mm	0.08/0.08mm
0.5mm	Type III HDI	0.075mm	0.06/0.06mm
≤0.4mm	Type III/IV HDI	0.05mm	0.05/0.05mm

Materials for HDI

Dielectric Materials

Standard Materials

- FR-4: Most common, good performance
- High-Tg FR-4: For high-temperature applications
- Low-Dk FR-4: For high-speed applications

Advanced Materials

- Rogers: For RF/microwave
- Megtron: For high-speed digital
- Isola: Low-loss materials
- Polyimide: For extreme environments

Impedance Control

Single-ended Impedance

Microstrip Impedance Formula:

$$Z0 = (87 / \sqrt{\varepsilon r + 1.41}) \times \ln(5.98h / (0.8w + t))$$

Stripline Impedance Formula:

$$Z0 = (60 / \sqrt{\varepsilon r}) \times \ln(4h / (0.67\pi(w + t)(0.8 + t/h)))$$

Where:

- Z0 = Characteristic impedance
- εr = Dielectric constant
- h = Dielectric thickness
- w = Trace width
- t = Trace thickness

Target Impedances

- Single-ended: 50Ω (most common)
- Differential USB: 90Ω
- Differential PCIe: 85Ω
- Differential Ethernet: 100Ω

Signal Integrity

High-Speed Considerations

Frequency-Dependent Losses

- Dielectric Loss: Material-dependent
- Copper Loss: Surface roughness effect
- Radiation Loss: Improper termination

Via Stubs

- **Problem**: Signal reflections from stubs
- **Solution**: Back-drilling or microvias
- **Benefit**: Improved signal integrity

Design for Manufacturing (DFM)

Design Rules

Minimum Feature Size

- Follow manufacturer's capabilities
- Include appropriate tolerances
- Consider yield implications

Panel Utilization

- Optimize board size for standard panels
- Consider array configuration
- Include tooling holes and fiducials

Documentation

Fabrication Notes

1. Material specifications
2. Layer stack-up details
3. Impedance requirements
4. Controlled impedance traces
5. Special requirements (via fill, etc.)

Best Practices Summary

Design

1. Use appropriate HDI type for application
2. Follow manufacturer's DFM guidelines
3. Consider manufacturability early
4. Include test points for verification
5. Document special requirements clearly

References: IPC-2226, IPC-6016, IPC-6012