HDI Best Practices

HDI PCB Design Best Practices

Overview

High-Density Interconnect (HDI) PCBs represent cutting-edge technology enabling smaller, faster, and more powerful electronic devices.

Core Design Principles

1. Layer Stack-Up Planning

- Use sequential lamination for complex designs
- Implement 1+N+1 or 2+N+2 stack-up structures
- Place signal layers adjacent to reference planes
- Symmetrical stack-up to minimize warpage

2. Microvia Design (2025 Standards)

- Diameter: ≤150 µm for standard HDI, ≤100 µm for ultra-HDI
- Aspect ratio: ≤1:1 for reliability
- Limit depth to 1-2 layers maximum
- Pad size: 0.25-0.30mm

3. Via-in-Pad Technology

- Direct laser drilling on component pads
- Copper plating and planarization
- Essential for BGAs with pitch ≤0.8mm

4. Trace Width and Spacing

- Minimum: 2 mil (0.05mm)
- Controlled impedance requires precise geometry
- Differential pairs: match lengths within 5 mil

5. DFM Guidelines

- Consult manufacturer for capabilities
- Provide detailed stack-up specifications
- Design for electrical testability

Applications

- Consumer electronics (smartphones, wearables)
- High-performance computing
- Medical devices
- Aerospace and defense

Based on industry best practices from AllPCB, Tessolve, and Cadence