

# HDI Via Design: Comprehensive Guide

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## Overview

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Vias are critical interconnects in HDI PCBs, connecting layers and enabling high-density routing. This guide covers via design, types, dimensions, and best practices for HDI applications.

## Via Types in HDI

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### Through-Hole Vias (Traditional)

#### Characteristics

- **Diameter:** 0.3mm - 0.6mm typical
- **Aspect Ratio:**  $\leq 10:1$
- **Connection:** Through entire board
- **Limitation:** Consumes routing space

### Blind Microvias

#### Definition

Connect an outer layer to one or more inner layers without going through the entire board.

#### Characteristics

- **Diameter:** 0.075mm - 0.15mm (3-6 mil)
- **Depth:** One or more layers
- **Aspect Ratio:**  $\leq 1:1$  recommended
- **Process:** Laser-drilled or mechanically drilled

#### Benefits

- Space savings
- Improved signal integrity (shorter path)
- Better for high-frequency signals
- Reduced stub effects

## Buried Vias

### Definition

Connect inner layers without extending to outer layers.

### Characteristics

- **Diameter:** 0.15mm - 0.25mm
- **Depth:** Between inner layers
- **Process:** Created during lamination
- **Visibility:** Not visible from outer layers

## Stacked Microvias

### Definition

Multiple microvias aligned vertically, connecting multiple layers.

### Design Rules

1. **Alignment:** Precise registration required
2. **Fill:** Typically filled with conductive or non-conductive material
3. **Plating:** Continuous plating through stack
4. **Reliability:** Lower than staggered vias

## Staggered Microvias

### Definition

Offset microvias in adjacent layers, connected through traces.

Benefits

- **Reliability:** Better than stacked
- **Manufacturing:** Easier than stacked
- **Cost:** Similar to stacked

## Via Dimensions and Specifications

Standard HDI Via Sizes

| Via Type          | Drill Size | Finished Hole | Pad Diameter | Land   | Aspect Ratio |
|-------------------|------------|---------------|--------------|--------|--------------|
| Laser Microvia    | 0.075mm    | 0.10mm        | 0.20mm       | 0.25mm | ≤1:1         |
| Small Microvia    | 0.10mm     | 0.125mm       | 0.25mm       | 0.30mm | ≤0.8:1       |
| Standard Microvia | 0.15mm     | 0.18mm        | 0.30mm       | 0.35mm | ≤0.8:1       |

## Via-in-Pad Design

Benefits

Electrical

- **Reduced Inductance:** Shorter path
- **Improved Signal Integrity:** Minimized stubs
- **Better High-Frequency Performance:** Less impedance discontinuity

Mechanical

- **Space Savings:** No escape routing needed

- **Smaller Footprint:** Enables tighter component placement
- **Better for Fine Pitch:** Essential for <0.5mm pitch BGAs

## Design Process

### 1. Via Drilling

- Use laser drilling for small vias
- Ensure proper location accuracy
- Maintain minimum distance from pad edge

### 2. Plating

- Standard copper plating (25µm minimum)
- Ensure good coverage
- Verify plating quality

### 3. Fill Materials

#### Conductive Epoxy Fill

- Silver-filled epoxy
- Improves thermal conductivity
- Provides electrical path
- Used for thermal or ground vias

#### Non-Conductive Epoxy Fill

- Dielectric material
- Provides planar surface
- Does not conduct electricity
- Used for signal vias

# Via Current Capacity

## Approximation Formula

For external vias with 10°C rise:

$$I = 0.8 \times d^{1.3}$$

Where:

- I = Current in amps
- d = Via diameter in mils

## Via Current Capacity Table

| Finished Hole Size | 10°C Rise | 20°C Rise | 30°C Rise |
|--------------------|-----------|-----------|-----------|
| 0.15mm (6 mil)     | 0.7A      | 1.0A      | 1.3A      |
| 0.20mm (8 mil)     | 1.0A      | 1.4A      | 1.8A      |
| 0.25mm (10 mil)    | 1.4A      | 1.9A      | 2.4A      |
| 0.30mm (12 mil)    | 1.7A      | 2.4A      | 3.0A      |

## Multiple Vias for High Current

- Use multiple vias in parallel
- Space evenly for current sharing
- Consider thermal relief

# Common Via Design Mistakes

| Mistake                   | Impact                     | Solution                                 |
|---------------------------|----------------------------|------------------------------------------|
| Insufficient annular ring | Breakout, poor reliability | Follow IPC minimums                      |
| Poor aspect ratio         | Plating voids, opens       | Keep $\leq 1:1$ for microvias            |
| Inadequate clearance      | Shorts, spacing violations | Check design rules                       |
| Via stubs in high-speed   | Signal reflections         | Use microvias or back-drill              |
| No thermal relief         | Soldering issues           | Use thermal relief for plane connections |

**References:** IPC-2226, IPC-6016, IPC-6012, IPC-2152