Impedance Routing 2025: Complete Guide to Controlled Impedance Design

Overview

Controlled impedance routing is essential for high-speed digital circuits, RF applications, and any design where signal integrity is critical. This guide covers impedance calculation, routing techniques, and best practices for 2025.

What is Impedance?

Definition

Impedance (Z) is the total opposition to current flow in an AC circuit, combining resistance (R) and reactance (X).

Characteristic Impedance

The characteristic impedance (Z_0) of a transmission line is the ratio of voltage to current for a wave propagating along the line.

Why Control Impedance?

Signal Integrity

- Prevents signal reflections
- Minimizes overshoot and undershoot
- Reduces ringing and oscillations
- Maintains signal fidelity

Power Transfer

- Maximum power transfer occurs when impedances match
- Minimizes signal loss
- Optimizes performance

Types of Controlled Impedance

Single-Ended Impedance

Applications

- General signal routing
- Clock signals
- Address/data buses
- Most digital signals

Common Values

- 50Ω: Most common for RF and high-speed digital
- 75Ω: Video and RF applications
- Other: Application-specific

Differential Impedance

Applications

- USB (Universal Serial Bus)
- PCIe (PCI Express)
- Ethernet (RJ45)
- SATA
- HDMI
- DDR memory

Common Values

- 90Ω: USB 2.0/3.x
- 85Ω: PCIe
- 100Ω: Ethernet
- 100Ω: SATA
- Other: Application-specific

Differential vs. Single-Ended

Aspect	Differential	Single-Ended
Noise Immunity	Excellent	Moderate
EMI	Lower	Higher
Cost	Higher	Lower
Complexity	Higher	Lower
Power	Two signals	One signal

Transmission Line Types

Microstrip

Definition

A trace on the outer layer with a reference plane beneath.

Structure

```
Dielectric
--------------
Reference Plane (Ground or Power)
```

Impedance Formula

$Z_0 = (87 / \text{sqrt}(\varepsilon r + 1.41)) \times \ln(5.98h / (0.8w + t))$

Where:

- Z_0 = Characteristic impedance (Ω)
- εr = Dielectric constant of material
- h = Height of dielectric
- w = Trace width
- t = Trace thickness

Pros

- Easier to fabricate
- Lower impedance
- Better for moderate frequencies
- Easy to access for probing

Cons

- More EMI radiation
- Susceptible to external noise
- Not suitable for very high frequencies

Stripline

Definition

A trace sandwiched between two reference planes.

Structure

```
--------------
Reference Plane
Dielectric
```

```
Trace
Dielectric
Reference Plane
--------------
```

Impedance Formula

$Z_0 = (60 / \text{sqrt}(\varepsilon r)) \times \ln(4h / (0.67\pi(w + t)(0.8 + t/h)))$

Where:

- Z_0 = Characteristic impedance (Ω)
- εr = Dielectric constant
- h = Distance between planes
- w = Trace width
- t = Trace thickness

Pros

- Lower EMI
- Better noise immunity
- Suitable for very high frequencies
- Controlled impedance

Cons

- Harder to fabricate
- Higher impedance typically
- Not accessible for probing
- More expensive

Coplanar Waveguide

Definition

Signal trace with ground traces on same layer on both sides.

Structure

```
Ground Trace  Signal Trace  Ground Trace
--------------------------------------
Dielectric
Reference Plane
```

Applications

- RF circuits
- Microwave applications
- High-frequency designs
- Where precise impedance control needed

Impedance Calculation

Material Properties

Dielectric Constant (Dk or εr)

The ability of a material to store electrical energy in an electric field.

Material	Dk (Typical)	Application
FR-4 Standard	4.3-4.8	General purpose
FR-4 High-Speed	3.8-4.2	High-speed digital
Rogers RO4003C	3.38	RF/microwave
Rogers RO4350B	3.48	RF/microwave
Isola FR408HR	3.7-3.9	High-speed

Dissipation Factor (Df or tan δ)

Measure of signal loss in the material.

Material	Df (Typical)	Loss
FR-4 Standard	0.020	High loss at high frequency
FR-4 High-Speed	0.010-0.015	Moderate loss
Rogers RO4003C	0.0027	Low loss
Rogers RO4350B	0.0037	Low loss

Calculation Tools

Online Calculators

- Saturn PCB Design Toolkit
- EEWeb Impedance Calculator
- PCB Impedance Calculator
- Manufacturer-specific tools

PCB Design Software

- Altium Designer: Built-in impedance calculator
- Cadence Allegro: SI tools
- Mentor Graphics: HyperLynx
- KiCad: Built-in calculator
- Most tools: Integrated calculators

Design Guidelines

Microstrip Design Rules

Target 50Ω Single-Ended

For FR-4 (εr = 4.5) with 1 oz copper (t = 0.035mm):

Dielectric Thickness (h)	Trace Width (w)
0.1mm	0.18mm
0.2mm	0.38mm
0.3mm	0.58mm
0.4mm	0.79mm
0.5mm	1.0mm

Target 90Ω Differential

For FR-4 (εr = 4.5) with 1 oz copper (t = 0.035mm) and 0.2mm dielectric:

Trace Width	Trace Spacing	Differential Impedance
0.15mm	0.15mm	~90Ω
0.20mm	0.20mm	~85Ω
0.10mm	0.10mm	~95Ω

Stripline Design Rules

Target 50Ω Single-Ended

For FR-4 (εr = 4.5) centered between planes (h = total spacing/2):

Plane-to-Plane Spacing	Trace Width (w)
0.2mm	0.15mm
0.3mm	0.23mm
0.4mm	0.31mm
0.5mm	0.39mm

Routing Best Practices

General Routing

1. Maintain Constant Impedance

- Keep trace width constant
- Maintain constant distance to reference plane
- Avoid changing layers (if possible)
- If changing layers, use impedance-matched vias

2. Reference Planes

- Provide continuous reference plane
- Avoid splits in reference plane under traces
- Use stitching vias near layer transitions
- Maintain plane integrity

3. Avoid Discontinuities

- Smooth corners (45° or curved)
- No 90° corners

- Proper via selection
- Minimize layer changes

Differential Pair Routing

1. Length Matching

- Match lengths within tolerance
- Typical tolerance: 5-10 mils
- Use serpentine routing for matching
- Match within pair, not to other pairs

2. Spacing

- Maintain constant spacing
- Keep spacing consistent
- Avoid obstacles in pair
- Minimize layer changes

3. Symmetry

- Route symmetrically
- Keep equal distances to obstacles
- Use same via patterns
- Maintain symmetry throughout

4. Layer Changes

- Change both signals simultaneously
- Use paired vias
- Maintain spacing through vias
- Consider impedance discontinuities

Impedance Testing

Time Domain Reflectometry (TDR)

How It Works

- Sends fast edge down transmission line
- Measures reflections
- Displays impedance vs. distance
- Identifies impedance discontinuities

TDR Specifications

- Rise Time: < 35ps for high-impedance accuracy
- Resolution: < 1mm typical
- Accuracy: ±5-10% typical

Test Coupons

Purpose

- Verify impedance during fabrication
- Test representative traces
- Calibrate process
- Ensure quality control

Design

- Include on panel
- Use same layer stack
- Representative trace geometries
- Include various impedances

Common Impedance Issues

Issue	Cause	Solution
Reflections	Impedance mismatch	Match impedances properly
Ringing	Improper termination	Add proper termination
EMI	Poor return path	Provide solid reference plane
Crosstalk	Traces too close	Increase spacing
Loss	Wrong material or trace	Use lower-loss material

Advanced Topics

Via Stubs

Problem

- Via acts as transmission line stub
- Causes reflections at high frequencies
- Degrades signal integrity

Solutions

- Back-drilling: Remove unused portion of via
- Microvias: Smaller, shorter vias
- Via-in-pad: Eliminates stub completely

High-Speed Considerations

Frequency-Dependent Losses

- **Dielectric Loss**: Material property
- **Copper Loss**: Skin effect, surface roughness
- **Radiation Loss**: Improper termination or routing

Skin Effect

- Current flows on conductor surface at high frequencies
- Increases effective resistance
- More significant above 1 GHz
- Consider copper surface roughness

References: IPC-2141, IPC-2251, IPC-2221