High-Speed Impedance

High-Speed Impedance Control

Overview

Impedance control is critical for high-speed PCB design to ensure signal integrity and minimize reflections.

Key Concepts

1. Controlled Impedance Basics

Why Impedance Matters:

- Prevents signal reflections
- Maintains signal integrity
- Reduces EMI and crosstalk
- Ensures proper signal timing

Target Impedance Values:

- Single-ended: 50Ω (common), 75Ω (video)
- Differential: 90Ω, 100Ω (USB), 120Ω (PCIe)

2. Trace Geometry Control

Critical Parameters:

- Trace width
- Dielectric thickness

- Copper weight
- Dielectric constant (Dk)

Calculations:
- Use field solvers for accurate results
- Online calculators for estimates
- Manufacturer impedance calculators

3. Routing Best Practices

High-Speed Routing Rules:

- Solid reference planes under traces
- Avoid crossing split planes
- Maintain consistent spacing
- Minimize via transitions
- Use 45° or curved bends (not 90°)

Differential Pair Routing:
- Match lengths within 5-10 mil
- Maintain consistent spacing
- No components between pairs
- Minimize layer transitions

4. Via Considerations

Via Effects on Impedance:
- Vias create impedance discontinuities
- Stub lengths cause reflections
- Use via-in-pad for high-speed
- Consider back-drilling for long stubs

5. Material Selection

Dielectric Properties:

- FR-4: Dk ≈ 4.0-4.5 (general use)
- High-speed materials: Dk ≈ 3.0-4.0
- Low-loss materials for >5GHz

6. Testing and Validation

TDR Testing:

- Time Domain Reflectometry
- Verify impedance values
- Locate discontinuities
- Validate differential pairs

Design Checklist

- [ ] Calculate required impedance
- [ ] Select appropriate dielectric
- [ ] Determine trace width/spacing
- [ ] Plan reference planes
- [ ] Specify in fabrication notes
- [ ] Include impedance test coupon

References: High-Speed PCB Routing Practices, TI High-Speed Layout Guide, NASA High-Speed Design