IPC-2221: Generic Standard on Printed Board Design

Overview

IPC-2221 is the foundational standard for PCB design, providing comprehensive guidelines for the design of rigid printed boards and rigid flex printed boards. It serves as the master design standard with supplemental documents covering specific board types.

Scope and Application

Board Types Covered

- Rigid printed boards
- Rigid flex printed boards
- Single-sided, double-sided, and multilayer boards
- High-density interconnect (HDI) boards

Related Standards

- IPC-2222: Rigid Organic Printed Board Design
- IPC-2223: Flexible Printed Board Design
- IPC-2224: PCMCIA Addendum
- IPC-2225: Design Guide for IC Package Carrier Boards
- IPC-2226: Design Guide for High Density Interconnect (HDI)

Material Selection

Base Material Properties

Dielectric Materials

- FR-4: Standard glass-epoxy, Tg 130-140°C
- High-Tg FR-4: Improved thermal performance, Tg 170-180°C
- Rogers Materials: RF/microwave applications
- Polyimide: High-temperature applications
- PTFE: Low dielectric constant for high-frequency

Selection Criteria

1. Operating temperature requirements
2. Electrical performance needs
3. Mechanical stability requirements
4. Cost considerations
5. Manufacturing capabilities

Copper Foil Types

- Electrodeposited (ED): Standard for most applications
- Rolled Annealed (RA): Better for flexible and high-frequency
- Reverse Treated Foil (RTF): Enhanced adhesion for multilayer

Design Rules

Conductor Width and Spacing

Minimum Trace Width

Application	Minimum Width	Current Capacity
Signal	0.10mm (4 mil)	Low current
Power	Calculated	High current
External Layers	0.15mm (6 mil)	Standard
Internal Layers	0.10mm (4 mil)	Standard

Current Capacity Calculator

For external layers:
[
I = k cdot T^{0.725} cdot W^{0.725}
]

For internal layers:
[
I = k cdot T^{0.5} cdot W^{0.5}
]

Where:

- I = Current in amps
- T = Trace thickness in oz/ft^2
- W = Trace width in mils
- k = 0.048 (external), 0.024 (internal)

Clearance Requirements

Minimum Clearances

- Internal Layers: 0.10mm (4 mil)
- External Layers: 0.15mm (6 mil)
- High Voltage: Add 0.025mm per 10V above 50V

Conductor to Board Edge

- Unplated Edge: 0.5mm (20 mil) minimum
- Plated Edge: 0.65mm (25 mil) minimum
- Routing/Tolerance: Add additional 0.15mm (6 mil)

Hole Design

Through Holes

Hole Sizes

- Minimum Finish Hole Size: 0.20mm (8 mil)
- Aspect Ratio: ≤8:1 standard, ≤10:1 advanced
- Tolerance: ±0.10mm (4 mil) typical

Annular Ring

- External Layers: 0.15mm (6 mil) minimum
- Internal Layers: 0.10mm (4 mil) minimum
- Breakout: Not acceptable for Class 2/3

Vias

Standard Via Sizes

- Microvia: 0.10mm - 0.15mm (4-6 mil)
- Standard Via: 0.20mm - 0.30mm (8-12 mil)
- Large Via: >0.30mm (12 mil)

Via Types

- Through Via: Goes through entire board
- Blind Via: From outer layer to inner layer

- Buried Via: Between inner layers only
- Via-in-Pad: Plugged and filled for surface mounting

Layer Stack-up Design

Standard Stack-up Principles

Layer Count Guidelines

- 2-Layer: Simple, low-density designs
- 4-Layer: Standard with power/ground planes
- 6-Layer: Better signal integrity
- 8+ Layers: High-speed, high-density designs

Symmetry Requirements

- Stack-up must be symmetrical
- Even copper distribution
- Balanced dielectric thickness
- Prevents warpage during manufacturing

Power and Ground Distribution

Plane Design

- Solid Planes: Best for power distribution
- Split Planes: Multiple voltage levels
- Mixed Signals: Separate analog and digital planes
- Ground Pours: Fill unused areas on signal layers

Decoupling Placement

- Near ICs: Within 2-5mm of power pins

- Multiple Values: Different frequency ranges
- Via Connections: Short, direct paths

Impedance Control

Characteristic Impedance

Microstrip (External Layer)

[
Z_0 = ↟rac{87}{sqrt{epsilon_r + 1.41}} lnleft(↟rac{5.98h}{0.8w + t}
ight)
]

Stripline (Internal Layer)

[
Z_0 = ↟rac{60}{sqrt{epsilon_r}} lnleft(↟rac{4h}{0.67pi(w + t)(0.8 + ↟rac{t}{h})}
ight)
]

Where:

- Z_0 = Characteristic impedance
- εr = Dielectric constant
- h = Dielectric thickness
- w = Trace width
- t = Trace thickness

Target Impedances

- Single-ended: 50Ω (most common)
- USB: 90Ω differential
- PCIe: 85Ω differential
- Ethernet: 100Ω differential

EMI/EMC Considerations

EMI Control Techniques

Grounding

- Low Impedance: Solid ground planes
- Multiple Ground Vias: Reduce return path impedance
- Guard Traces: Protect sensitive signals
- Ground Fill: Reduce loop areas

Signal Routing

- Minimize Loop Areas: Reduces radiation
- Differential Pairs: Cancel EMI fields
- Reference Planes: Provide return paths
- Length Matching: For differential signals

Shielding Methods

- Copper Pours: On outer layers
- Shielding Cans: Metal enclosures
- Via Fences: Around sensitive circuits
- Board Edge Plating: Creates Faraday cage

Thermal Design

Heat Dissipation

Copper Thickness for Heat

- 1 oz: Standard, 35µm

- 2 oz: Improved, 70µm
- 3+ oz: High current/power

Thermal Relief

- Spoked Connections: Four connections typical
- Air Gaps: 0.25-0.5mm around pads
- Plane Connections: Multiple vias for heat transfer

Temperature Considerations

- Tg (Glass Transition): Maximum operating temperature
- CTE Mismatch: Expansion differences
- Thermal Vias: Conduct heat to inner layers or backside

Documentation Requirements

Fabrication Drawing

Required Information

1. Board dimensions and tolerances
2. Layer stack-up details
3. Material specifications
4. Copper weights per layer
5. Drill chart with sizes and tolerances
6. Surface finish specification
7. Solder mask and legend details
8. Special requirements

Assembly Drawing

1. Component placement coordinates

2. Reference designators
3. Polarity indicators
4. Special assembly notes
5. BOM (Bill of Materials)

Design for Manufacturability (DFM)

Design Guidelines

Panelization

- Rail Width: 10-15mm typical
- Spacing: 2-5mm between boards
- Tooling Holes: For manufacturing alignment
- Fiducials: For automated assembly

Test Points

- Accessible: On outer layers
- Spaced: 2.54mm grid preferred
- Size: 1.0mm minimum
- Location: Near critical test points

Cost Optimization

1. Minimize layer count
2. Use standard materials
3. Optimize board utilization
4. Specify appropriate tolerances
5. Design for standard drill sizes

Quality and Reliability

Design Verification

- DRC (Design Rule Check): Automated verification
- ERC (Electrical Rule Check): Netlist verification
- Signal Integrity Analysis: For high-speed designs
- Thermal Analysis: For power circuits

Testing Considerations

- Bed-of-Nails Test: Test points needed
- Flying Probe: Less restrictive test point requirements
- Boundary Scan: For BGA and high-density
- ICT (In-Circuit Test): Comprehensive test access

Industry Trends and Future Directions

Emerging Technologies

- High-Speed Design: 10+ Gbps data rates
- HDI and Microvias: Increasing density
- Embedded Components: Reducing board size
- Flexible Circuits: Wearable electronics
- Material Advances: Low-loss, high-Tg materials

Design Challenges

- Signal Integrity: Higher frequencies
- Power Integrity: Lower voltages, higher currents
- Thermal Management: Increased power density

- **Miniaturization**: Smaller form factors

Reference: IPC-2221 Standard

This guide provides essential design information. Always consult the official IPC-2221 standard for complete requirements.